Amendments to the Specification:

The paragraph on page 10, beginning at line 16, has been amended as follows:

The diode ring array 112 of FIG. 5A has been fabricated using the PHEMT technology where the minimum anode width W is 25 μm. It can be seen in FIG. 5A [[5]]that each diode has one finger (i.e., N = 1) with an anode gate finger width W, which can be 25 μm, for example. Since there are four diode rings 120 in the diode ring array 112, the total effective diode width W_{eff} for all anti-parallel diode rings connected between the connection point P and ground is: W_{eff} = R x (2 x N x W) = 4 x (2 x 1 x 25) μm = 200 μm . The effective diode size W_{eff} may of course be different in other embodiments, depending on the technology used, the number of diode rings, the width of each diode, and/or the like. In the parallel-connected diode ring array 112 of FIG. 4A, all diode rings are connected on one side to the connection point P. On the other side, the diode rings are electrically connected to via holes 128, which form the connection to ground.